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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
KIELIN, ERIK J	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 27

Application Number: 09/346,436
Filing Date: July 01, 1999
Appellant(s): HOUSTON, THEODORE W.

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Jay M. Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 23 October 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief. (See Brief filed 10 July 2001, Paper no. 15.)

(2) Related Appeals and Interferences

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. (See Brief filed 10 July 2001, Paper no. 15.)

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. (See Substitute Supplemental Appeal Brief filed 4 November 2002, Paper no. 23.)

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. (See Brief filed 10 July 2001, Paper no. 15.)

(5) Summary of Invention

The summary of invention contained in the brief is correct. (See Brief filed 10 July 2001, Paper no. 15.)

(6) Issues

The appellant's statement of the issues in the brief is correct. (See Substitute Supplemental Appeal Brief filed 4 November 2002, Paper no. 23.)

(7) Grouping of Claims

Appellant's brief includes a statement that claims 9 and 22 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8). (See Substitute Supplemental Appeal Brief filed 4 November 2002, Paper no. 23.)

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct. (See Substitute Supplemental Appeal Brief filed 4 November 2002, Paper no. 23.)

(9) Prior Art of Record

US 5,087,585 Hayashi 2-1992

Appellant's admitted prior art

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7, 9, and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by US 5,087,585 (**Hayashi**).

Regarding claim 7, Hayashi discloses a method of fabricating an SOI structure comprising:

providing a substrate **13, 21, 22** (Fig. 2B), with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. the "first layer device" **22**);

providing a device wafer **14, 15, 23**, with a planar surface, having at least one of active or passive elements on a surface thereof (i.e. "second layer thin film device" **23**);

forming a substantially planar region on said surface of said device layer and said surface of said substrate (shown in Fig. 2B);

forming a substantially planar region on said surface of said electrically insulating layer (shown in Fig. 2B);

interposing said electrically insulating layer **17** between said device layer and said substrate **13, 21, 22** with said planar region of said electrically insulating layer **17** overlaying said substantially planar region on said at least one of said surface of said device layer **14, 15, 23** and said surface of said substrate **13, 21, 22** to make and electrical contact with a device in at least one of the device wafer and the substrate **13, 21, 22** (col. 5, lines 11-15; Fig. 2B); and

then bonding said planar surface of said electrically insulating layer **17** to said overlying one of said substrate **13, 21, 22** and said device layer **14, 15, 23** (shown in progression from Fig. 2B to Fig. 2C).

Note that on page 7, lines 5-7 the instant specification, layer **5** is referred to as the "device layer 5" which is shown only as a layer in the instant figures **without** any specific "passive" or "active" elements shown. Compare to either of **22** or **23** in Fig. 2B of Hayashi, as noted above, which shows the same nondescript "first layer device" or "second layer thin film device" without any passive or active elements shown. Accordingly, the "active" and "passive" elements are shown to the same extent in both the instant specification and Hayashi.

Regarding claim 9, the method of claim 7 further comprising an electrically insulating layer **17** having an electrical interconnect structure **18** therewithin, said interconnect structure 18 contacting both said device layer **14, 15, 23** and said substrate **13, 21, 22**.

Regarding claim 18, Hayashi discloses a method of fabricating an integrated circuit comprising:

(a) providing a device layer **23** having active or passive elements (i.e. devices) thereon (Fig. 2B);

(b) providing a substrate **21** having active or passive elements (i.e. devices **22**) thereon (Fig. 2B);

(c) providing a dielectric **17** bonded to one of said device layer and said substrate having an interconnect **18** disposed therein and extending to at least one surface thereof (Fig. 2B); and

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface (shown in Fig. 2C) with said one of said device layer and said substrate **13, 21, 22** and forming an electrically conductive path across said interface to said interconnect (shown in progression from Fig. 2B to Fig. 2C).

See also columns 3-4, and see column 5, lines 11-16.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 stands rejected under 35 U.S.C. 103(a) as being unpatentable over **Hayashi** in view of Appellant's admitted prior art (**APA**).

Hayashi, as indicated above, discloses all of the features of the instant invention except for (1) stating that a dielectric layer forms over the interconnect structure **18** thereby preventing electrical conduction; or (2) applying a voltage across the dielectric layer to break down said the dielectric layer to establish an electrical connection.

On page 7, lines 7-12, **APA** states that it is known in the art (1) for native oxide (a dielectric) to form on metal interconnect, and (2) to breakdown oxide by applying voltage across an electrically insulating layer (e.g. a native oxide) by stating,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art.**" (Emphasis added; specification page 7, lines 7-12.)

Accordingly, it is seen to be inherent that a native oxide (i.e. dielectric layer preventing electrical conduction) forms on the interconnect structure **18** of **Hayashi**, because **APA** admits that this is known to occur. Moreover, it must be known that the oxide would form; otherwise, one would not know to remove it or how to remove it. As further support, it may be implicit in **Hayashi** alone that a native oxide dielectric exits on the non-refractory metal pool **18** and on the refractory metal bump **13**, because **Hayashi** indicates that the bonding step is carried out until the refractory metal bump "cuts into" the metal pool to establish electrical contact (col. 5, lines 25-31). Apparently, then, the physical contact alone between **18** and **13** generated upon bringing the substrate **13**, **21**, **22** and the insulating layer **17** together for bonding (Figs. 2B to 2C) is insufficient to create **electrical** contact.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a voltage across the dielectric of **Hayashi** device to breakdown the native oxide on **18** and **13** thereby improving and/or ensuring an electrical connection in the **Hayashi** interconnect between **18** and **13**, as suggested by **APA** and as desired in **Hayashi**.

*(11) **Response to Argument***

At present, as best understood by Examiner, all issues have been withdrawn by Appellant except those directed to claims 9 and 22. Examiner is not certain which arguments require addressing in the numerous Briefs presented by Appellant. Accordingly, the arguments directed to claims 9 and 22 will be addressed as presented in the original Appeal Brief (Paper no. 15), the Reply Brief filed 18 October 2001 (Paper no. 17), and the latest Substitute Supplemental Appeal Brief (Paper no. 23), Paper no. 23 appearing to be a duplicate of Paper no. 19. The arguments presented in the original Appeal Brief incorporate arguments from claims 1 and 7 into claims 9 and 22. Accordingly, the arguments directed to claims 1 and 7 will also be addressed.

Appeal Brief (Paper no. 15) arguments directed to claims 9 and 22

In the Appeal Brief, beginning on p. 5, Applicant argues,

> "Claim 7 requires, among other steps, provision of an SOI structure having a device layer having at least one of active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof and an electrically insulating layer having an interconnect structure disposed within the electrically insulating layer and extending to a surface of the electrically insulating layer. No such step is taught or suggested by Hayashi either alone or in the combination as claimed as discussed above with reference to claim 1."
>
> "Claim 7 further requires the steps of forming a substantially planar region on the surface of the device layer and the surface of the substrate

> and a region on the surface of the electrically insulating layer, interposing the electrically insulating layer between the device layer and the substrate with the planar region of the electrically insulating layer overlaying the substantially planar region on the at least one of the surface of the device layer and the surface of the substrate to make electrical contact with a device in at least one of the device wafer and the substrate and then bonding the surface to the other of the substrate wafer and device layer." No such steps are taught or suggested by Hayashi either alone or in the combination as claimed."

As stated in the original Examiner's Answer (Paper no. 16), Appellant has done nothing more than restate claim 7 and allege that the features --which Examiner clearly pointed out to be in Hayashi-- are simply not there. No argument has been provided for Examiner to address since Examiner clearly pointed out the location in Hayashi wherein each of these features can be found. Examiner refers the Board to the rejection of the claims above. Appellant then continues,

> "Note the argument presented in connection with claim 1 as well as the fact that Hayashi has no electrically insulating layer having an interconnect structure which provides the claimed interconnect function in the electrically insulating layer bonded to one of the device layer or substrate after being affixed to the other of these elements in the manner claimed."

Again, Examiner clearly pointed out in Hayashi that the interconnect structure **18** is shown to be **in** the insulating layer **17** in Fig. 2B. For whatever reason, Appellant still contends that **18** is not "in" **17**. Examiner remains perplexed, given the clear showing in Hayashi.

Since claims 1 and 7 are "canceled" it is unclear to what extent the arguments presented regarding claim 1 are incorporated into the arguments regarding claims 9 and 22, Examiner will address these arguments just in case they are considered to be incorporated into the arguments regarding claims 9 and 22. Accordingly, regarding claim 1, Appellant argues beginning on p. 3 of the Appeal Brief,

> "The substrate or device layer is then planarized along with the exposed surface of the dielectric layer and the exposed surface and the substrate or device layer are then bonded together after being aligned."

No planarization step or aligning step is claimed or even mentioned in claim 1. Claim 7 requires only "forming a substantially planar **region** on said surface of said device layer and said surface of said substrate" (emphasis added) which are clearly shown in Fig. 2B of Hayashi, as pointed out in the rejection of the claims. The bonding step is shown in progression from Figs. 2B to 2C in Hayashi. Like claim 1, claim 7 makes **no** mention of aligning.

The Appeal Brief continues on p. 3, "There is no build-up of layer upon layer as is found in Hayashi." This is an irrelevant argument because (1) no such limitation is claimed, (2) no such limitation is implicit in the claim language, and (3) the instant invention --in fact-- only provides for building up layer upon layer, in direct contradiction to the argument presented in the Appeal Brief that no such "build-up" occurs. The instant specification at page 8, lines 8-9, states, "One option is to form the dielectric 3 in layers with **multiple levels of interconnect** 11 as illustrated in FIGURE 3." (Emphasis added.) The instant specification at page 8, lines 8-9, states, "Various dielectric materials or composites thereof can be used to form layer 3, such as, for example, **grown** oxides, **deposited** oxides, and nitrides." (Emphasis added.) Instant claim 1 states, "forming an electrically insulating layer having a pair of opposed outer faces...**on said surface** of one of said substrate or said device wafer." (Emphasis added.) In each of the aforementioned instances, **a dielectric layer is formed upon another layer** (either the device wafer or the substrate) -- not to mention "multiple levels of interconnect." This is very clearly "build-up of layer upon layer" and is also no different from what Hayashi does in Figs. 1D to 1E wherein a dielectric layer **17** is formed upon the device layer **16**. For these reasons, the arguments

presented in the Appeal Brief in this regard are contradictory and irrelevant as being drawn to un-claimed limitations.

The Appeal Brief presents the argument, on page 3, last paragraph, "Furthermore, the interconnect is disposed within the dielectric layer. No such arrangement is found in Hayashi." Similarly, Appeal Brief presents on page 4, first full paragraph, "There is no interconnect in Hayashi and, in the event the non-refractory metal pool **18** is alleged to be such interconnect, which it is not, this element is not disposed within the insulative layer **17**." Examiner respectfully disagrees noting that Appeal Brief's statements clearly contradict the teachings of the applied art. The refractory metal pool is --in fact-- interconnect both by definition and by its explicit use in Hayashi. Hayashi, column 3, lines 49-53, states "A non-refractory metal is filled to the opening formed in the rear insulative layer **17** so as to form, as an undersurface connection electrode, a non-refractory metal pool **18**..." Furthermore, and perhaps more importantly, Hayashi states in column 5, lines 11-15, "Furthermore, it would be apparent that the present invention can be applied to **stacking** of devices formed on semiconductor substrates other than a silicon substrate and **also of wiring layers formed on insulative substrates**." (Emphasis added.) This statement demonstrates that Hayashi **also** intends the use of his method for forming multiple levels of wiring layers **in** the insulating layer **17** (i.e. "multiple levels of interconnect" as coined in the instant specification). Hayashi uses the non-refractory metal pool to form a single or multiple wiring layers **in** the insulating layer **17** for electrical connections between devices on different layers (device layers **22**, **23**). The refractory metal pool **18** is therefore, by definition, interconnect, because it forms electrical connections between separate devices. It is also necessarily "disposed within the insulative layer" to every extent instantly claimed. The non-

refractory metal pool **18** is explicitly shown and stated to be within the dielectric layer **17**. The explicit use and showing of interconnect **18** disposed within an insulative layer **17**, clearly shows arguments presented in the Appeal Brief to be without a basis in fact.

Beginning with the last sentence on page 3, Appeal Brief presents the argument,

> "Still further, any insulation buildup between the interconnect and the device in the substrate to which interconnection is to be made is obviated by the application of a sufficiently high voltage across the insulation buildup, **when necessary**, between the interconnect and the device in the substrate to break down the intervening insulation and provide contact between the interconnect and the device in the substrate of device layer. It follows that the structures of Hayashi and the subject invention and the method of fabrication of the two are entirely different and unrelated to each other." (Emphasis added.)

The issue of the incidental, unintentional build-up of dielectric material which impedes the electrical interconnect is **not** rejected under Hayashi **alone**, but is instead rejected under Hayashi in view of Appellant's admitted prior art (APA), as noted above in the rejection. Since the Brief has ventured the argument presently and has not addressed it at all in its appropriate location under "ISSUE 2," it will be addressed here.

In as much as the build-up of dielectric (e.g. native oxide) (1) may be incidental, (2) is ultimately broken down to eliminate it, and (3) is **admitted prior art**, Appellant's use of this limitation as the distinguishing novelty is highly suspect. Claim 22 simply does not distinguish between the incidental and intentional formation of a dielectric layer on the interconnect. As repeated from the rejection above, on page 7, lines 7-12 of the instant specification, it is stated to be known in the art for the incidental formation to occur and to break down incidental build-up of insulative or dielectric material by applying voltage across the electrically insulating layer. In this regard, the specification states,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art.**" (Emphasis added; specification page 7, lines 7-12.)

No further addressing of this argument is deemed necessary because the claims presently rejected under Hayashi **alone** (claims 7, 9, and 18) do **not** have this limitation. Nonetheless, Appellant clearly provides the appropriate suggestion to use such a known method.

Regarding the remainder of page 4 of the Brief's arguments which are directed to claim 1, The Brief restates without argument that Hayashi lacks (1) the formation of the "electrically insulating layer with a pair of opposed outer faces...disposed on one of the substrate or the device wafer;" (2) the interconnect structure (**18** in Hayashi) extending substantially to the one of the outer faces of the electrically insulating structure (**17** in Hayashi) to make electrical contact with a device (either **22**, or **23** in Hayashi) in at least one of the device wafer and the substrate, but each of these features is clearly shown in Hayashi as indicated in the rejections above.

Further in this regard, the Brief presents the argument,

> "The pool of Hayashi is not disposed at a surface of the electrically insulating structure and is not shown as being connected to anything in the second layer thin film device 23 other than the layer itself."

Examiner notes with interest that this is exactly how Appellant has portrayed the instant interconnect (as noted in the rejection above) in the instant figures, with the interconnect connected to nothing but the device layer itself. (See device layer 5 and interconnect 7 in instant Figures 1-3. It is therefore, improper for the Brief posit a distinction between the present invention and Hayashi on the basis of the very same thing that is absent in Appellant's own

disclosure. Nonetheless, "interconnect" is used for electrically connecting devices (hence the name); it is not randomly strewn on or in a semiconductor device without purpose. Its art known purpose renders the actual showing of the devices themselves unnecessary, as clearly intended by the equivalent absence in Appellant's own figures. Therefore, the argument forwarded in the Appeal Brief is not persuasive.

Beginning in the last sentence of page 4, the Brief argues that Hayashi teaches a different order of steps. Examiner is perplexed. Figures 1D to 1E of Hayashi show the formation of the insulative layer **17** with the interconnect **18** contacting the device layer **16** so this order of steps is taught. In progression from Figures 2B to 2C in Hayashi, the substrate is next bonded to the device wafer. The Hayashi figures clearly show the same order of steps as claimed by Appellant. Examiner does not know what else to say.

This concludes the rebuttal of the arguments presented in the Appeal Brief (Paper no. 15) regarding claims 1 and 7, which may or may not be incorporated into the arguments regarding claims 9 and 22.

With regard to claim 9, the Appeal Brief presents the argument,

> "Claim 9 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting **both** the device layer and the substrate. The argument applied as to claim 8 applies herein as well." (Emphasis added.)

The argument presented in regard to claim 8 states,

> "In addition, claim 8 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting **at least one** of the device layer and the substrate. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The interconnect structure

> of Hayashi is not "**in** the electrically insulating layer" but rather is external thereto." (Emphasis added.)

As noted above several times, **18** is the interconnect structure formed in the insulating layer **17**. The interconnect **18** is shown to contact **both** the device layer **23** and the substrate **13, 21, 22** at the surface of **13**. **Nowhere** is **18** (the interconnect or "refractory metal pool") shown to be **external** to the insulation layer **17** in Hayashi. Again, Examiner is perplexed as to how Appellant could continue to maintain this argument that the interconnect **18** is somehow "**external**" to the insulating layer **17** in **direct contradiction** to that shown in the Hayashi figures. Accordingly, each feature is taught and the Brief presents no argument as to why the features indicated in the rejection to be shown in Hayashi somehow do not meet the claim limitations.

Further in this regard, the Appeal Brief presents the argument at p. 8, last paragraph,

> "With reference to the Examiner being perplexed as to the position of appellant as to the interconnect 18 of Hayashi, this is a metal pool and is not at the surface of the interconnect to which reference is being made. The metal pool 18 of Hayashi is disposed **in** an aperture **in** a layer 17 and is otherwise unrelated to the layer 17 in any way. This structure does not read on that which is being claimed." (Emphasis added.)

For whatever reason, Appellant contradicts himself regarding the location of the interconnect **18** of Hayashi. After previously indicating --as noted just above-- that the interconnect **18** is "external" to the insulating layer, Appellant contradictorily states --now in agreement with Examiner-- "[t]he metal pool 18 of Hayashi is disposed **in** an aperture **in** a layer 17."

With regard to claim 22, the Appeal Brief (Paper no. 15) presents the argument,

> "Claim 22 further limits claim 18 by requiring that the step of forming an electrically conductive path across the interface to the interconnect be formed by breakdown of the dielectric. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof."

Claim 22 introduces a **different** "dielectric" from that "dielectric" in claim 18 so it is unclear as to which dielectric Appellant is referring in this argument. Furthermore, claim 22 is not rejected over Hayashi alone, but is instead rejected over Hayashi in view of APA, as the rejections have always made clear. Note that it has been held that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Because claim 22 depends from claim 18, and because Examiner is unsure if Appellant intends the arguments regarding claim 18 to be incorporated into the arguments regarding claim 22, the arguments regarding claim 18 as presented in the Appeal Brief will now be addressed. The Appeal Brief presents the argument with regard to claim 18,

> "Claim 18 requires, among other steps, after providing a device layer having at least one of active or passive elements on a surface thereof and providing a substrate having at least one of active or passive elements on a surface thereof, providing a dielectric bonded to one of the device layer and the substrate having an interconnect disposed therein and extending to at least one surface thereof. No such step is taught or suggested by Hayashi either alone or in the combination as claimed."
>
> "Claim 18 further requires the step of then bonding the dielectric to the other of the device layer and the substrate to form an interface with the one of said device layer and the substrate and form an electrically conductive path across the interface to the interconnect. No such step or steps in the order claimed are taught or suggested by Hayashi."

As with the arguments directed to claim 7, the Brief has done nothing more that restate claim 18 and simply alleged that each of these features is absent from Hayashi **without** any argument as to why that indicated in the rejection to be in Hayashi does not meet the claim limitation. Examiner refers the Board to the rejection of the claims above.

This concludes the rebuttal of arguments presented in the Appeal Brief (Paper no. 15).

Reply Brief (Paper no. 17) arguments directed to claims 9 and 22

The Reply Brief presents the argument that the electrical interconnect structure does not contact both the device layer and the substrate in Hayashi, stating,

> "The interconnect structure of Hayashi is the metal pool which does not contact both the device layer and the substrate. This contact is only later made when the refractory metal bump later contacts the metal pool. Accordingly, the order of the steps as specifically claimed in the combination of claims 7 and 9 is not met by Hayashi."

As noted above, in the rejection of the claims, Hayashi shows said contact. There exists no requirement in claims 7 or 9 as to when such contact is made or as to what type of contact, the claim limitation "contact" is directed. As shown in Fig. 2C of Hayashi, the 18 is in physical contact with 13, and as stated in Hayashi, electrical contact is made. This is all that is required in claims 7 and 9. Moreover, the electrically insulating layer **17** having an electrical interconnect structure **18** therewithin, said interconnect structure **18** contacting **both** said device layer **14, 15, 23** --at **23**-- and said substrate **13, 21, 22** --at **13**. Accordingly, all claim limitations are met.

Further in this regard, the interconnect structure **18** of Hayashi (the metal pool) does, in fact, contact both the substrate and the device layer. Without such contact no electrical connection could exist, therefore contact is made. If it is thought that the refractory metal bump **13** is not part of either the device layer then this may be a difference, but the Hayashi Figures (Fig. 2A for example) clearly show the refractory metal bump **13** to be part of a substrate **21, 22** inasmuch as it is used to electrically interconnect the devices in layer **22** to via refractory metal pool **18** to the device layer **23**. If it is thought that the interconnect structure of Hayashi (the

metal pool **18**) does *not* contact the substrate because there is another intervening device layer (item 22 in Fig. 2B of Hayashi), then this might be a difference, **but in pertinent points**, (1) the instant claims claim the presence of passive and active devices formed **on** a surface of each of the substrate and the device layer; (2) the instant Fig. 1 shows the device layer **5** to be formed **on** a substrate; and (3) the instant specification states on page 6, lines 6-8,

> "The device wafer 5 and the substrate 1 may have active and/or passive devices formed therein and optionally **making a connection to an interconnect in the electrically insulating layer**." (Emphasis added.)

Therefore, the **instant specification** (1) explicitly defines both the "device wafer" and the "substrate" to include "devices" which is identical to the substrate and device wafer of Hayashi show in Figs. 2A and 2B, as each have devices; and (2) **implicitly defines the refractory metal bump 13 to be part of the device layer,** by using the phrase, "optionally making a connection to an interconnect in the electrically insulating layer" because the refractory metal bump **13** makes a connection to the "interconnect in the electrically insulating layer." Accordingly, the statements presented in the Brief contradict the instant specification in indicating that the interconnect structure **18** of Hayashi does not contact both the device wafer and the substrate.

The Reply Brief also argues, in the last sentence of page 1,

> "Accordingly, the order of the steps as specifically claimed in the combination of claims 7 and 9 is not met by Hayashi."

The only order claimed in claims 7 and 9 is found in claim 7 wherein claim 7 recites the limitation, "then bonding" after the interposing step which makes electrical connection by bringing the devices together. The instant specification states in the section entitled, "Summary of the Invention" at p. 4, beginning at line 5,

> "In each case, optionally, a thin dielectric layer may be formed between an interconnect structure and the bonding interface, either inadvertently or to facilitate bonding. Then a sufficiently high voltage is applied across this thin dielectric to cause breakdown and **completion of the interconnection**. The voltage can be applied at any point **after the bonding**, including immediately **after bonding**, **after** device wafer thinning, **after** initial patterning of the device layer, and **after** packaging of the completed integrated circuit." (Emphasis added.)

Accordingly, there exists no support for the alleged order of steps argued in the Reply Brief since the specification specifically requires the electrical connection be made **after --not before--** the bonding step. This argument applies equally to the order presented in claim 18 as well, since claim 18 claims the same order as in claim 7. Hayashi specifically teaches this order of bonding then connecting by stating that the substrate and insulating layer are "bonded to each other until the refractory metal bump **13** formed on the first layer thin film device layer **22** cuts into and electrically contacts with the non-refractory metal pool **18**..." (Hayashi; col. 4, lines 25-35).

Regarding page 2 of the Reply Brief, the argument is presented,

> "As to claim 22, there is no so-called admission in Appellant's APA that it is even known that the oxide will appear in **the process as claimed**, let alone that it be known to remove such oxide, especially in the environment claimed." (Emphasis added.)

It is respectfully submitted that this argument is wholly without merit. First, and as pointed out in the rejections and restated here for convenience, the instant specification states,

> "In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, **a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or the other dielectric** and allow completion of the connection **as is well known in the art**." (Emphasis added; specification page 7, lines 7-12.)

The instant specification explicitly states that the instant process leads to the formation of thin native oxide because Appellant is describing the instant invention at the cited location in the instant specification. Moreover, it begs the question as to how one of ordinary skill would know to remove the oxide if no oxide were known to form on the metal in the first place. Therefore, it must be known that the oxide would form; otherwise, one would not know to remove it or how to remove it. Regarding the "claimed environment," there is no claimed environment, so this issue is moot. Accordingly, the points at issue in claim 22 is clearly admitted prior art.

This concludes the rebuttal of the arguments presented in the Reply Brief (Paper no. 17) regarding claims 9 and 22.

Substitute Supplemental Appeal Brief (Paper no. 23) arguments directed to claims 9 and 22

The Supplemental Brief presents arguments beginning at page 2, line 4, arguing that Examiner has made an invalid argument that "[m]erely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable." Examiner excerpted 37 CFR 1.192(c)(7) (1995) which states,

> "For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. **Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable**." (Emphasis added.)

This argument was provided to point out that Appellant has not presented an argument as to why claims 9 and 22 stood separately from their independent claims 7 and 18, respectively. This argument is moot because only claims 9 and 22 are active. Accordingly, this argument is not directed to an appealable issue because it is not directed to why claims 9 and 22 patentably distinguish from Hayashi and Hayashi in view of APA.

The Supplemental Brief again argues that the interconnect structure **18** is not formed in the insulating layer **17** in Hayashi. Examiner already responded to this argument above.

The Supplemental Brief again argues that the interconnect structure **18** does not contact both the substrate and the device layer. Examiner already responded to this argument above.

The Supplemental Brief again argues that the order presently claimed is not taught in Hayashi. Examiner already responded to this argument above and re-iterates the only order argued is not supported by the instant specification.

The Supplemental Brief again argues that the incidental formation of oxide over the interconnect and the breakdown by applying a voltage is not APA. Examiner already responded to this argument above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Erik Kielin, Ph. D.
February 13, 2004

Conferees at the Appeal Conference held on 20 January 2004.

Carl Whitehead, Jr., Supervisory Patent Examiner

O. C.
Olik Chaudhuri, Supervisory Patent Examiner

Erik Kielin, Primary Patent Examiner

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265